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(71) Applicant *(for all designated States except US)*: **CANON KABUSHIKI KAISHA** [JP/JP]; 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo 146-8501 (JP).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **MATSUDA, Yojiro** [JP/JP]; 228-2-A201, Manpukuji, Asao-ku, Kawasaki-shi, Kanagawa 215-0004 (JP).

(74) Agent: **YAMADA, Ryuichi**; Toko International Patent Office, Hasegawa Bldg. 4F, 7-7, Toranomon 3-chome, Minato-ku, Tokyo 105-0001 (JP).

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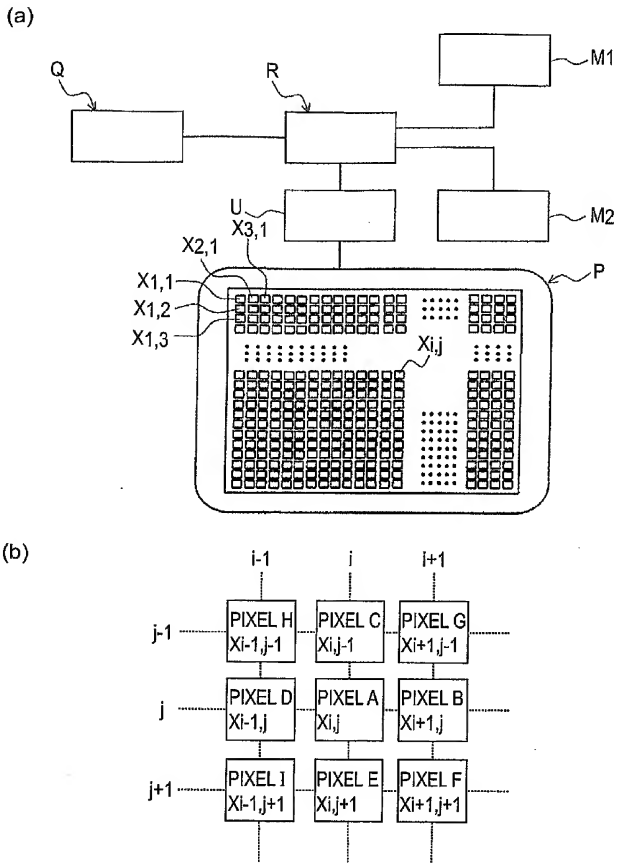
(54) Title: DISPLAY APPARATUS



(57) Abstract: In a display apparatus using charged electrophoretic particles, being controlled by an electric field at the pixels,in some cases the charged particles fail to display a desired gradation level even when a voltage is applied to the pixel with the intention of providing the desired gradation level. In such cases, correction values for all the gradation levels are obtained in advance by experiment, and then a corrected voltage is applied to the pixel, whereby it is possible to provide a desired gradation by compensating an influence of an electric field at adjacent pixels.

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DESCRIPTION

DISPLAY APPARATUS

[TECHNICAL FIELD]

The present invention relates to a display apparatus which includes a plurality of pixels arranged in a matrix and effects gradation display at each pixel.

[BACKGROUND ART]

In recent years, as a display device for displaying various information, an electrophoretic display device for displaying information by controlling a position of electrophoretic particles (charged migration particles) or a liquid crystal display device for displaying information by applying a voltage to a liquid crystal has received attention.

These display devices are constituted by a matrix of pixels each at which gradation display can be effected.

Figures 12(a) and 12(b) are respectively a sectional view showing an example of a structure of a conventional electrophoretic display device described in Japanese Laid-Open Patent Application (JP-A) No. 2000-258805. This electrophoretic display device includes a pair of substrates 21a and 21b provided

with electrodes 24a and 24b, respectively. In a spacing between the substrates 21a and 21b, a dispersion liquid 22 and electrophoretic particles 23 are disposed. The dispersion liquid 22 and the electrophoretic particles 23 have been colored different colors. As shown in Figure 12(a), in the case where the electrophoretic particles 23 are attracted to the electrode 24a side, the color (e.g., black) of the dispersion liquid 22 is visually identified as the color of the pixels. On the other hand, as shown in Figure 12(b), in the case where the electrophoretic particles 23 are attracted to the electrode 24b side, the color (e.g., white) of the electrophoretic particles 23 is visually identified as the color of the pixels. Further, in the case where the electrophoretic particles 23 are stopped in an intermediary portion between the substrates 21a and 21b, a halftone is displayed.

Although there arises no particular problem in the case where voltages at adjacent pixels (pixels A and B) are equal to each other as shown in Figures 12(a) and 12(b) or provides a small difference therebetween, in the case where the voltage difference between the adjacent pixels is larger a shown in Figure 13, arrangement of the electrophoretic particles at a boundary portion C between the adjacent pixels are disordered by an electric field

interference between the adjacent pixels. As a result, an original gradation cannot be provided to impair a display quality in some cases.

[DISCLOSURE OF THE INVENTION]

An object of the present invention is to provide a display apparatus which effectively suppresses a deterioration in display quality.

According to the present invention, there is provided a display apparatus, comprising:

a display device comprising a plurality of pixels arranged in a matrix,

a drive circuit for outputting a gradation signal to each of the pixels, and

a correction circuit for correcting the gradation signal at each pixel so that a desired gradation can be provided by compensating an influence from adjacent pixels.

This and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

[BRIEF DESCRIPTION OF THE DRAWINGS]

Figure 1(a) is a block diagram showing a

general structure of the display apparatus according to the present invention, and Figure 1(b) is a schematic view showing an arrangement of pixels.

Figure 2 is a view showing an example of a relationship between gradation level, a gradation signal, and a display gradation (reflectance), at a pixel.

Figure 3 is a view showing an example of a relationship between a gradation level, a gradation signal, and a display gradation (reflectance), in the case where an identical gradation is provided at a correction pixel and adjacent pixels.

Figure 4(a) is a view showing a relationship between a combination of display gradations at a correction pixel and adjacent pixels (left column), a display gradation (reflectance) at the correction pixel in the case where correction is not made (central column), and a gradation signal for displaying an appropriate gradation at the correction pixel (right column), in the case where the gradation level at the correction pixel is 4; and Figure 4(b) is a view showing a relationship between a combination of display gradations at a correction pixel and adjacent pixels (left column), a display gradation at the correction pixel in the case where correction is not made (central column), and a gradation signal for displaying an appropriate gradation at the correction

pixel (right column), in the case where the gradation level at the correction pixel is 8.

Figure 5(a) is a view showing a relationship between a combination of display gradations at a correction pixel and adjacent pixels (left column), a display gradation (reflectance) at the correction pixel in the case where correction is not made (central column), and a gradation signal for displaying an appropriate gradation at the correction pixel (right column), in the case where the gradation level at the correction pixel is 5; and Figure 5(b) is a view showing a relationship between a combination of display gradations at a correction pixel and adjacent pixels (left column), a display gradation at the correction pixel in the case where correction is not made (central column), and a gradation signal for displaying an appropriate gradation at the correction pixel (right column), in the case where the gradation level at the correction pixel is 16.

Figures 6 and 7 are respectively a flow chart for explaining a progress of data processing by a correction circuit.

Figures 8(a), 8(b), 9(a), 9(b), 10(a) and 10(b) are respectively a sectional view for explaining a drive state of an electrophoretic display device.

Figures 11(a), 11(b) and 11(c) are respectively a sectional view for explaining a drive

state of a liquid crystal display device.

Figures 12(a) and 12(b) are respectively a sectional view showing an embodiment of a structure of a conventional electrophoretic display device.

Figure 13 is a sectional view for illustrating a conventional problem.

[BEST MODE FOR CARRYING OUT THE INVENTION]

Hereinbelow, embodiments of the present invention will be described with reference to Figures 1 to 11.

(1) First, a general structure of a display apparatus will be described.

A display apparatus according to the present invention, as shown in Figures 1(a) and 1(b), includes a display device P having a plurality of pixels X1, 1, ... arranged in a matrix, a drive circuit Q for outputting a gradation signal to each of the pixels X1, 1, ..., and a correction circuit R correcting the gradation signal for each pixel so as to permit a desired gradation display by compensating an influence from adjacent pixels. In a preferred embodiment, the drive circuit Q outputs digital image data, and the correction circuit R corrects the digital image data depending on a characteristic of the display device P. Between the correction circuit R and the display device P, a circuit U which penetrates an analog

signal for driving the display device P may preferably be disposed.

A display gradation may be controlled by: (a) a method wherein a magnitude of a voltage applied to each pixel is controlled in such a display device P that a display gradation is changed depending on a magnitude of the applied voltage (so-called "voltage modulation"); (b) a method wherein a period (length) of time of application of a voltage to each pixel is controlled in such a display device P that a display gradation is changed depending on a length of application time (so-called "pulse width modulation"; and (c) a method wherein both a magnitude of and a length of application of a voltage applied to each pixel are controlled in such a display device P that a display gradation is changed depending on both the magnitude of the applied voltage and the length of application of the applied voltage.

In the case of (a) and (c), the gradation signal comprises a signal for determining a magnitude of the applied voltage, and in the case of (b) and (c), the gradation signal comprises a signal for determining a length (period) of voltage application time.

(2) THe correction circuit R will be described.

Assuming that only one pixel is virtually driven, as shown in Figure 2, a gradation (level) 1

(GRADATION 1) is provided when the drive circuit Q applies a gradation signal V1. Similarly, a gradation 2 is displayed under application of a gradation signal V2, and a gradation x is displayed under application of a gradation signal Vx.

However, a relationship between the gradation signal Vx and the display gradation x at a pixel is not an absolute one, so that the display gradation x is changed under the influence of adjacent pixels surrounding the pixel when other pixels are also driven. (This will be described more specifically later.) In the case of Figure 2, the gradation signal is a voltage signal. However, a similar problem arises in the case of the gradation signal comprising the signal for determining the length of voltage application time.

The correction circuit R is constituted so that it corrects a gradation signal applied to each pixel to compensate an influence from its adjacent pixels, thus providing a desired gradation at the pixel.

Herein, in case of necessity, a pixel at which a gradation signal is corrected by the above described correction circuit is referred to as a "correction pixel", and pixels disposed adjacent to the correction pixel are referred to as "adjacent pixels".

In the case where a pixel A (PIXEL A) shown in Figure 1(b) is to be corrected, the influence on the pixel A from its adjacent pixels (e.g., pixels B, C, D and E) is compensated by the correction circuit R. Accordingly, in this case, the correction pixel is the pixel A and the adjacent pixels are the pixels B, C, D and E. Further, in the case where the pixel B is to be corrected, the influence on the pixel B from its adjacent pixels (e.g., pixels G, A, F, ...) is compensated by the correction circuit R. Accordingly, in this case the correction pixel is the pixel B, and the adjacent pixels are the pixels G, A, F, ...

In the case where pixels are arranged in rows and columns as shown in Figure 1(b), the number of pixels adjacent to the correction pixel A is 8, i.e., the pixels H, C, G, B, F, E, I and D, so that a gradation signal may be corrected with the assumption that all the eight pixels are the adjacent pixels but the correction of the gradation signal in the present invention is not particularly limited thereto. For example, the gradation signal may be corrected with the assumption that only four pixels B, C, D and E (upper, lower, left and right pixels) are the adjacent pixels or with the assumption that only two pixels D and B (left and right pixels) are the adjacent pixels. In the case where there is a pixel which is largely affected by electric field interference between

adjacent pixels, correction to the gradation signal may preferably be made in view of the pixel.

In order to effect such a correction by the correction circuit R, the correction circuit R is required to obtain a gradation signal to be applied to a correction pixel on the basis of input of information on a gradation to be displayed at the correction pixel (e.g., pixel A) and input of information on a gradation to be provided at adjacent pixels (e.g., pixels B, C, D and E).

The correction of the gradation signal on the basis of inputted information may be made by the following methods.

A relationship between states of adjacent pixels (e.g., gradations (gradation levels) to be provided at adjacent pixels B, C, D and E, as shown in the left column of Figures 4(a), 4(b), 5(a) and 5(b)), a gradation (gradation level) to be provided at a correction pixel (e.g., a gradation to be provided at the correction pixel A, as shown in the left column of Figures 4(a), 4(b), 5(a) and 5(b)), and a gradation signal applied to the correction pixel so as to permit a desired gradation display at the correction pixel (e.g., the gradation signal as shown in right column of Figures 4(a), 4(b), 5(a) and 5(b)), is prepared in advance as table data and a gradation signal to be applied to the correction pixel is obtained on the

basis of the relationship between the state of the adjacent pixels and the gradation to be provided at the correction pixel. It is also possible to use a method wherein a gradation signal to be applied to the correction pixel is obtained by substituting states of adjacent pixels and a gradation to be provided at the correction pixel into a formation for calculation obtained in advance through experiment.

In the former method, the table data may preferably be obtained in advance through experiment and stored in a nonvolatile storing device (nonvolatile memory) (e.g., as indicated by a symbol M1 in Figure 1(a); hereinafter referred to as a "first memory"), and the correction circuit R may preferably obtain a gradation signal to be applied to the correction pixel on the basis of data stored in the first memory M1.

(3) Hereinafter, the above described table data will be described in detail with reference to Figures 2 to 5.

Here, a relationship between a gradation signal and a display gradation (reflectance) in the case of driving only the pixel A (correction pixel) is shown in Figure 2.

This relationship is not changed even when the adjacent pixels B, C, D and E are driven at the same gradation as the correction pixel A (Figure 3).

However, in the case where there is a large difference between a gradation to be provided at the adjacent pixels and a gradation to be displayed at the correction pixel, the resultant gradation displayed at the correction pixel is deviated under the influence of the adjacent pixels.

For example, in the case where a gradation (level) 4 is provided at the correction pixel A, all the combinations of display gradations at the adjacent pixels B, C, D and E are shown in the left column in Figure 4(a), and a gradation (exactly a reflectance as a parameter corresponding to a gradation of a reflection type display device) when a gradation signal V4 which has not been corrected is applied to the correction pixel A, is shown in the central column in Figure 4(a). As shown in Figure 4(a), in the combinations of display gradations indicated by a symbol K11, the desired gradation 4 (reflectance = 17 %) is displayed at the correction pixel A by applying the gradation signal V4. However, in the combinations indicated by a symbol K12, the resultant gradation (brightness) is somewhat low (dark) compared with the case of the combinations of K11. Further, in the case where a gradation (level) 8 is provided at the correction pixel A, all the combinations of display gradations at the adjacent pixels B, C, D and E are shown in the left column in Figure 4(b), and a

gradation when a gradation signal V8 which has not been corrected is applied to the correction pixel A, is shown in the central column in Figure 4(b). As shown in Figure 4(b), in the combinations of display gradations indicated by a symbol K22, the desired gradation 8 (reflectance = 33 %) is displayed at the correction pixel A by applying the gradation signal V8. However, in the combinations indicated by a symbol K21, the resultant gradation (brightness) is somewhat high (bright) compared with the case of the combinations of K22. Further, in the combinations indicated by a symbol K23, the resultant gradation is somewhat dark.

Further, in the case where a gradation (level) 12 is provided at the correction pixel A, all the combinations of display gradations at the adjacent pixels B, C, D and E are shown in the left column in Figure 5(a), and a gradation when a gradation signal V12 which has not been corrected is applied to the correction pixel A, is shown in the central column in Figure 5(a). As shown in Figure 5(a), in the combinations of display gradations indicated by a symbol K32, the desired gradation 4 (reflectance = 49 %) is displayed at the correction pixel A by applying the gradation signal V12. However, in the combinations indicated by a symbol K31, the resultant gradation (brightness) is somewhat high (bright)

compared with the case of the combinations of K32. Further, in the case where a gradation (level) 16 is provided at the correction pixel A, all the combinations of display gradations at the adjacent pixels B, C, D and E are shown in the left column in Figure 5(b), and a gradation when a gradation signal V16 which has not been corrected is applied to the correction pixel A, is shown in the central column in Figure 5(b). As shown in Figure 5(b), in the combinations of display gradations indicated by a symbol K42, the desired gradation 16 (reflectance = about 65 %) is displayed at the correction pixel A by applying the gradation signal V16. However, in the combinations indicated by a symbol K41, the resultant gradation (brightness) is somewhat high (bright) compared with the case of the combinations of K42.

In this embodiment, the phenomena as described with reference to Figures 4(a), 4(b), 5(a) and 5(b) and correction values (V4' in Figure 4(b), V8 and V8" in Figure 4(b), V12' in Figure 5(a), and V16' in Figure 5(b)) for displaying a desired (predetermined) gradation (level) are experimentally obtained in advance with respect to all the gradations and are tabulated. The correction circuit R described above corrects the gradation signal by making reference to the resultant table.

(4) Next, a specific procedure of the correction

of gradation signal will be described with reference to Figures 6 and 7.

First, flags i and j are set to 1 (S1 in Figure 6) and gradations (e.g., pixel data) to be provided at a correction pixel Xi,j and its adjacent pixels Xi+1,j; Xi,j-1; xi-1,j; and Xi,j+1 are extracted (S2 in Figure 6). In this case, the relationships: $i-1 \geqq 1$ and $j-1 \geqq 1$ must be satisfied. In this regard, pixels Xi,j-1 and Xi-1,j are actually not present in the case of $i = j = 1$, and accordingly a necessary processing is effected.

Then, by making reference to the table data or the like, a gradation signal (e.g., a valve of rewriting voltage) to be applied to the correction pixel Xi,j is calculated (S3 in Figure 6). The calculated result may preferably be stored in a second storing device (memory) M2 shown in Figure 1(a). Then, i is changed from 1 to 2 while retaining j (= 1) as it is (S4, S5 and S6 i Figure 6), and a gradation signal for a correction pixel X2, 1 is calculated (S2 and S3 in Figure 6). After the gradation signals for the pixels arranged in rows are calculated, a gradation signal for a second row pixel is calculated by setting $i = 1$ and $j = 2$ (S4, S5 and S7 in Figure 6). At the time of calculated a gradation signal for the last row pixel, calculation of gradation signals is completed (S4 in Figure 6).

At that time, the gradation signals for all the pixels are stored in the second memory M2 etc., and the signals are sent to the display device to display an image.

After the data processing shown in Figure 6, data processing shown in Figure 7 may be effected. More specifically, as shown in Figure 7, after the gradation signals (rewriting voltages) for all the pixels are calculated as described above, the calculation results (calculated gradation signals) for the correction pixel Xi,j and the adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1 are extracted (S12), and a gradation signal (e.g., a value of rewriting voltage) to be applied to the correction pixel Xi,j is calculated by making reference to table data etc. (S13). This processing is effected similarly with respect to all the pixels (S14, S15, S16 and S17).

Such a calculation for all the pixels may be effected not only once but also plural times (S18 and S19). An accuracy of correction is improved as the number of such a calculation is increased.

In this case, the table data to which reference is to be made are not those shown in Figures 4 and 5 (i.e., with respect to the relationship between the display gradations and the correction gradation signals) but those with respect to a

relationship between gradation signals (e.g., rewriting voltages) calculated through data processing, shown in Figure 6, for the pixels Xi,j; Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1, and a correction gradation signal for the correction pixel Xi,j.

The correction of the gradation signal by the correction circuit R may preferably be made in the case where a deviation of the display gradation is out of a predetermined range. For example, in the case where a deviation ratio (= {(a gradation provided by a gradation signal which has not been corrected)/(a gradation to be provided)} x 100) is within a predetermined acceptable range (e.g., less than ±3 % in terms of an absolute value), the data processing shown in Figure 6 may be omitted. The gradation provided by the correction shown in Figures 6 and 7 may not be necessarily completely identical to that to be provided originally but may have an error which is within the predetermined acceptable range. In other words, a variation in reflectance is not necessarily required to become zero by making the correction. For example, it is sufficient to make the correction so as to provide a reflectance variation of less than ±1 % (in terms of an absolute value). Accordingly, a rewriting voltage conversion table is prepared by calculating a correction value with respect to a gradation signal providing a reflectance variation of

not less than ±1 % (in terms of an absolute value). Such an experiment may generally preferable be performed by an automatic measuring system. Further, the correction of rewriting voltage may preferably be made on the basis of magnitude (amplitude) of applied voltage, a length of voltage application time, voltage application timing, etc.

(5) Next, the display device will be described.

As the display device P, a display device which includes a plurality of pixels arranged in a matrix and is capable of effecting gradation display at each pixel, can be used. For example, the display device P may include the electrophoretic display device (e.g., P1 shown in Figure 8(a)) for displaying various information by moving electrophoretic particles 3, and the liquid crystal display device (e.g., P2 shown in Figure 11(a)) for displaying various information by applying a voltage to a liquid crystal 13.

Hereinafter, the respective structures of the electrophoretic display device and the liquid crystal display device will be described more specifically.

(5-1) Structure of electrophoretic display device

The electrophoretic display device P1 may include, as shown in Figures 8(a), 8(b), 9(a), 9(b), 10(a) and 10(b), a pair of substrates 1a and 1b disposed opposite to each other with a spacing, a

plurality of electrophoretic particles (charged migration particles) 3 and a dispersion liquid 2 which are disposed in the spacing, and a pair of electrodes 4a and 4b which are disposed close to the dispersion liquid 2. The electrophoretic display device may preferably be driven according to an active matrix driving scheme by connecting a switching device, such as a thin film transistor (TFT) onto one of the electrodes (e.g., the electrode 4a). The electrophoretic display device may further be connected with a power source, a timing controller, a D/A converter, a shift register, etc. The electrophoretic display device may also be driven according to a generally known passive matrix driving scheme.

The electrophoretic display device P1 described above may preferably be of a reflection-type. A structure and a driving method for the reflection type electrophoretic display device will be described below.

In the reflection-type electrophoretic display device, the electrodes 4a and 4b are disposed to sandwich the dispersion liquid 2 therebetween, and the dispersion liquid 2 and the electrophoretic particles 3 may preferably be colored different colors. In the following description, for convenience of explanation, the dispersion liquid 2 is colored

black and the electrophoretic particles are colored white.

Such a reflection type electrophoretic display device P1 may be driven by the voltage modulation method as follows.

(a) As shown in Figures 8(a) and 2, when the electrode 4a is supplied with a voltage V1 = -10 V while keeping the electrode 4b at 0 V, the electrophoretic particles 3 are stopped at a position L1 along the electrode 4a to provide a gradation (level) 1.

(b) As shown in Figures 8(b) and 2, when the electrode 4a is supplied with a voltage V4 = +2 V, the electrophoretic particles 3 are stopped at a position L2 to provide a gradation 4.

(c) As shown in Figures 9(a) and 2, wherein the electrode 4a is supplied with a voltage V11 = +7 V, the electrophoretic particles are stopped at a position L3 to provide a gradation 11.

(d) As shown in Figures 9(b) and 2, when the electrode 4a is supplied with a voltage V16 = +10 V, the electrophoretic particles are stopped at a position L4 to provide a gradation 16.

Similar gradation display may be performed by also the pulse width modulation method.

In Figures 8(a), 8(b), 9(a) and 9(b), the same voltage is applied to the electrode 4a at

adjacent pixels A and B, so that a desired gradation can be provided without correcting the gradation signal. However, as shown in Figures 10(a), when the applied voltages to the adjacent pixels A and B are different from each other, an electric field interference between the adjacent pixels is caused to occur. As a result, the electrophoretic particles in the vicinity of a pixel boundary are disordered (e.g., an electric field at a portion C is affected by a voltage applied to the pixel B disposed adjacent to the pixel A) to cause deviation of display gradation. More specifically, when all the electrophoretic particles in the vicinity of the pixel boundary are stopped at the position L2 as shown in Figure 8(b), the gradation 4 can be provided. However, a part of the electrophoretic particles 3 is moved toward the substrate 1a side, so that the resultant display gradation becomes somewhat darker. More specifically, a resultant reflectance at the gradation 4 should be originally 17 % but an actual reflectance was about 15 %>

Accordingly, as shown in Figure 10(b), the gradation signal is corrected from V4 (= +2.0 V) to V4' (= +2.5 V) to change the position of electrophoretic particles 3 from L2 to L2', thus realizing the gradation 4 (reflectance = 17 %).

In the electrophoretic display device P1, a

partition wall is provided between the adjacent pixels so as to suppress movement of the electrophoretic particles 3 at a pixel to another pixel adjacent to the pixel. Further, the dispersion liquid 2 and the electrophoretic particles 3 may preferably be sealed in a microcapsule 5. This microcapsule 5 may be provided in a position corresponding to each pixel. The position of the microcapsule, however, may not be aligned with the pixel. Further, it is also possible to dispose a plurality of microcapsules at one pixel.

(5-2) Structure of liquid crystal display device

As shown in Figures 11(a), 11(b) and 11(c), the liquid crystal display device may include a pair of substrates 11a and 11b disposed opposite to each other with a spacing, a liquid crystal layer 13 disposed in the spacing, and a pair of electrodes 14a and 14b disposed so as to sandwich the liquid crystal layer 13. Of the electrodes 14a and 14b, one electrode 14b may be a common electrode connected in common with all the pixels and the other electrode 14a may be a pixel electrode for each pixel. The common electrode is grounded (to have a voltage of 0 V) and a rewriting voltage applied to the pixel electrode is changed, whereby it is possible to effect switching of display mode.

In the case where the liquid crystal display device is of a reflection type, the rear electrode 14a

may preferably be formed of a metal having a high reflectance so as to function as a reflection layer.

As shown in Figures 11(a) and 11(c), when the same voltage is applied to both the adjacent pixels A and B, it is possible to provide an appropriate gradation. However, as shown in Figure 11(b), when voltages applied to the adjacent pixels A and B are different from each other, an alignment state of liquid crystal is disordered at a pixel boundary portion C, thus causing deviation of display gradation. For this reason, the applied voltage to the pixel A is corrected to obviate the deviation of display gradation.

(6) Capacities of the memories M1 and M2 are not particularly restricted, and as the memories M1 and M2, it is possible to use a line memory, a frame memory, etc.

According to the embodiment described above, it is possible to provide a desired gradation (level) by compensating an influence on the correction pixel from its adjacent pixels.

Examples

Hereinbelow, the present invention will be described more specifically based on Examples.

(Example 1)

A display apparatus shown in Figures 1(a) and 1(b) was prepared in the following manner. The

display apparatus included, as a display device P, an electrophoretic display device P1, as shown in Figures 8(a) and 8(b) having a matrix of pixels with 300 rows and 250 columns.

The electrophoretic display device P1 included a pair of 1.1 mm-thick glass substrates 1a and 1b. In a spacing between these substrates 1a and 1b, a plurality of microcapsules 5 each containing a dispersion liquid 2 and electrophoretic particles 3 were prepared through a composite coacervation method and disposed. The dispersion liquid 2 was colored black with a dye, and the electrophoretic particles 3 were formed of white titanium oxide. A electrode 4b on an observer (viewer) side ("common electrode") was formed of transparent ITO (indium tin oxide), and an opposite electrode 4a ("pixel electrode") was formed of Al (aluminum). Further, to each of the pixel electrodes 4a, a TFT (not shown) was connected so as to permit frame rewriting by an active matrix driving scheme.

From a drive circuit Q, digital image data were outputted. In a correction circuit R, the digital image data were corrected depending on a characteristic of the display device. In an analog signal generating circuit U, a digital signal was converted into an analog signal.

In the correction circuit R, data processing

as shown in Figure 6 was performed. The display apparatus in this example effects 4 bit-gradation display at each pixel. The image data comprises digital information providing 4 bit-gradation at each pixel. When the inputted image data are not 4 bit-gradation data, they are converted into 4 bit-gradation data.

First, referring again to Figure 6, i = 1 and j = 1 are set (S1), and values of image data for a correction pixel Xi,j and its adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1 are extracted from a memory (S2). THen, by making reference to table data (rewriting voltage conversion table data), a rewriting voltage for the correction pixel Xi,j is calculated (S3). The thus calculated rewriting voltage (digital information providing a voltage value) is stored in the second memory M2.

Thereafter, checking of "i = 250 and j = 300" is arrived out (S4), and in the case of "No", checking of "i = 250" is carried out (S5). However, as described above, i = j = 1, so that i = i+1 is set (S6). The extraction (S2) and the calculation of rewriting voltage (S3) are performed in the same manner as described above.

Similar processing is repeated, and at such a stage that image data for 250 pixels X1,1; X2,1; X3,1; ... X250,1 are sequentially extracted

completely, i is 250 and j is 1, so that i is set to 1 and j is set to 2 (S4, S5 and S7). Thereafter, image data for 250 pixels X1,2; X2,2l X3,2; ... X250,2 are extracted. Similarly, image data are extracted after the value of j is changed to 3, 4, 5, ... 300.

When a rewriting voltage value for the last pixel x250,300 is determined, i is 250 and j is 300, so that the data processing is completed (S4).

Next, the rewriting voltage conversion table used in this example will be described.

The rewriting voltage conversion table was prepared through an experiment with an automatic measuring system while paying attention to the correction pixel Xi,j and its adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1 in the display apparatus having the matrix with 300 rows and 250 columns.

First, a reference at the correction pixel Xi,j when the same rewriting voltage was applied to the correction pixel Xi,j and the adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1, and a reflectance at the correction pixel Xi,j when a first rewriting voltage was applied to the correction pixel Xi,j and a second rewriting voltage which was different from the first rewriting voltage, was applied to the adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi-1,j, were obtained.

Next, in the case where a difference between

these reflectances (i.e., a variation in reflectance) was not less than ±2 % (in terms of an absolute value), the rewriting voltage for the correction pixel Xi,j was corrected so that the later reflectance was less than ±2 % (in terms of an absolute value) on the basis of the former reflectance. The correction of rewriting voltage was performed by changing the magnitude of applied voltage and/or the length of voltage application time and/or the voltage application timing. In the above described manner, with respect to all the combinations of rewriting voltages providing a reflectance variation of not less than ±2 % (as an absolute value), correction values were obtained to prepare a rewriting voltage conversion table.

After the correction of digital image data by the correction circuit R, an analog signal for driving the display device was generated in the analog signal generating circuit U and the rewriting voltage was applied to the display device having the matrix with 300 rows and 250 columns.

As a result, it was possible to effect 16 gradation (level) display at each pixel with a variation within ±2 % on the basis of a desired reference for each gradation (level).

(Example 2)

In this example, rewriting voltages for all

the pixels were determined in the same manner as in Example 1 by using the same apparatus as in Example 1, and were stored in a memory.

The data processing shown in the flow chart of Figure 7 was performed.

More specifically, i = 1, j = 1 and k = 1 are set (S11), and values of the rewriting voltages for a correction pixel Xi,j and its adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1 were extracted from the memory (S12).

Next, a rewriting voltage for the correction pixel Xi,j is obtained by making reference to table data (S13). The obtained rewriting voltage value is digital information providing a voltage value, which is stored in a predetermined memory.

Then, when "i = 250 an j = 300" are not satisfied, checking of "i = 250" is carried out (S14 and S15). In the case where "i = 250" is not satisfied, i = i+1 and j = j are set (S15 and S17), and a correction value of rewriting voltage is obtained (S12 and S13). This data processing is repeated until "i = 250 and j = 300" are satisfied, whereby new (correction) values of rewriting voltage for all the pixels (300x250 matrix) are determined (S14).

Next, checking of "k = 3" is carried out and when "k = 3" is not satisfied, i = 1, j = 1 and k =

k+1 are set. Thereafter, the above described sequence of data processing is repeated.

After all, with respect to all the pixels, the correction of rewriting voltage is made three times (k = 1, 2 and 3) to complete the data processing.

Next, the rewriting voltage conversion table used in this example will be described.

The rewriting voltage conversion table was prepared through an experiment with an automatic measuring system while paying attention to the correction pixel Xi,j and its adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1 in the display apparatus having the matrix with 300 rows and 250 columns.

First, a reference at the correction pixel Xi,j when the same rewriting voltage was applied to the correction pixel Xi,j and the adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi,j+1, and a reflectance at the correction pixel Xi,j when a first rewriting voltage was applied to the correction pixel Xi,j and a second rewriting voltage which was different from the first rewriting voltage, was applied to the adjacent pixels Xi+1,j; Xi,j-1; Xi-1,j; and Xi-1,j, were obtained.

Next, in the case where a difference between these reflectances (i.e., a variation in reflectance) was not less than ±1 % (in terms of an absolute

value), the rewriting voltage for the correction pixel Xi,j was corrected so that the later reflectance was less than ±1 % (in terms of an absolute value) on the basis of the former reflectance. The correction of rewriting voltage was performed by changing the magnitude of applied voltage and/or the length of voltage application time and/or the voltage application timing. In the above described manner, with respect to all the combinations of rewriting voltages providing a reflectance variation of not less than ±1 % (as an absolute value), correction values were obtained to prepare a rewriting voltage conversion table.

After the correction of digital image data by the correction circuit R, an analog signal for driving the display device was generated in the analog signal generating circuit U and the rewriting voltage was applied to the display device having the matrix with 300 rows and 250 columns.

As a result, it was possible to effect 16 gradation (level) display at each pixel with a variation within ±2 % on the basis of a desired reference for each gradation (level).

(Example 3)

In this example, a display apparatus shown in Figure 1 including a liquid crystal display device P2 shown in Figure 11 was prepared.

As a pair of substrates 11a and 11b, a 1.1 mm-thick glass substrate was used. An electrode 14b on an observer side was formed of transparent ITO and an opposite electrode 14a was formed of Al. Other structural members and data processing were the same as those in Example 1.

As a result, according to this example, it was possible to effect display at an appropriate gradation.

[INDUSTRIAL APPLICABILITY]

As described hereinabove, according to the present invention, it is possible to provide a desired gradation by compensating an influence on a pixel from its adjacent pixels in a display apparatus using an electrophoretic display device or a liquid crystal display device.

CLAIMS

1. A display apparatus, comprising:

a display device comprising a plurality of pixels arranged in a matrix,

a drive circuit for outputting a gradation signal to each of the pixels, and

a correction circuit for correcting the gradation signal at each pixel so that a desired gradation can be provided by compensating an influence from adjacent pixels.

2. An apparatus according to Claim 1, wherein the plurality of pixels include a correction pixel at which a gradation signal is corrected by said correction circuit and adjacent pixels surrounding the correction pixel, and said correction circuit obtains a gradation signal, to be corrected, on the basis of information on a gradation to be provided at the correction pixel and information on a gradation to be provided at the adjacent pixels.

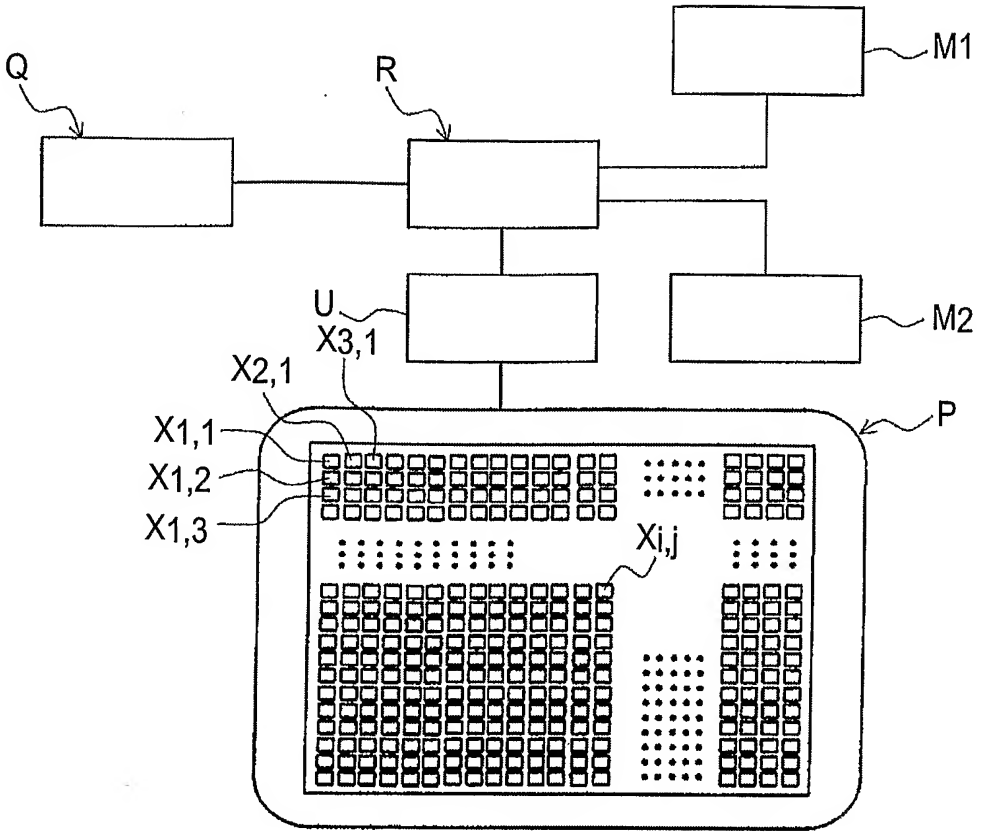
3. An apparatus according to Claim 2, wherein said apparatus further comprises a first storing device which stores a relationship between states of the adjacent pixels, a gradation to be provided at the correction pixel, and a gradation signal to be applied

to the correction pixel so as to provide a desired gradation at the correction pixel, said correction circuit obtaining the gradation signal to be applied to the correction pixel on the basis of data stored in the first storing device.

4. An apparatus according to Claim 1, wherein the correction of the gradation signal by the correction circuit is effected when a deviation ratio of a display gradation is out of a predetermined range.

5. An apparatus according to Claim 1, wherein the display device is an electrophoretic display device for displaying various information by moving charged electrophoretic particles or a liquid crystal display device for displaying various information by applying a voltage to a liquid crystal.

(a)


Q
R
M1
U
X3,1
M2
X2,1
P
X1,1
X1,2
X1,3
Xi,j

(b)

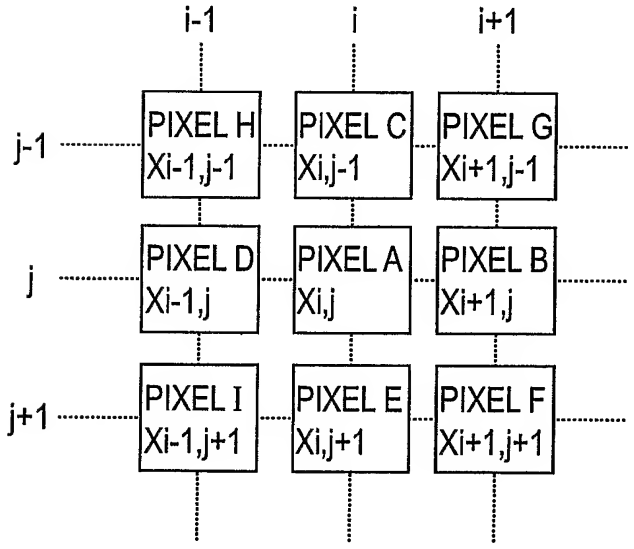

i-1
i
i+1
j-1
PIXEL H
Xi-1,j-1
PIXEL C
Xi,j-1
PIXEL G
Xi+1,j-1
j
PIXEL D
Xi-1,j
PIXEL A
Xi,j
PIXEL B
Xi+1,j
j+1
PIXEL I
Xi-1,j+1
PIXEL E
Xi,j+1
PIXEL F
Xi+1,j+1

FIG. 1

	GRADATION SIGNAL	REFLECTANCE OF PIXEL A
GRADATION 1	V_1 = -10V	5%
GRADATION 2	V_2 = 0.7V	9%
GRADATION 3	V_3 = 1.3V	13%
GRADATION 4	V_4 = 2V	17%
. . . .	. . . .	. . . .
GRADATION 14	V_{14} = 8.7V	57%
GRADATION 15	V_{15} = 9.4V	61%
GRADATION 16	V_{16} = 10V	65%

FIG. 2

	A B C D E	GRADATION SIGNAL OF PIXEL A	REFLECTANCE OF PIXEL A
GRADATION 1	1 1 1 1 1	V1	5%
GRADATION 2	2 2 2 2 2	V2	9%
GRADATION 3	3 3 3 3 3	V3	13%
GRADATION 4	4 4 4 4 4	V4	17%
	. . . .		. . . .
GRADATION 14	14 14 14 14 14	V14	57%
GRADATION 15	15 15 15 15 15	V15	61%
GRADATION 16	16 16 16 16 16	V16	65%

FIG.3

(a) GRADATION 4 AT PIXEL A

	A	B	C	D	E	REFLECTANCE	GRADATION SIGNAL
K11	4	1	1	1	1	17%	V4
	4	1	1	1	2	17%	V4
	4	1	1	2	2	17%	V4
	4	1	2	2	2	17%	V4
	4	2	2	2	2	17%	V4
	⋮					⋮	⋮
	4	7	7	7	7	17%	V4
	4	7	7	7	8	17%	V4
	4	7	7	8	8	16.9%	V4
	4	7	8	8	8	16.9%	V4
	4	8	8	8	8	16.8%	V4
	⋮					⋮	⋮
K12	4	15	15	15	15	15.2%	V4'
	4	15	15	15	16	15.2%	V4'
	4	15	15	16	16	15.1%	V4'
	4	15	16	16	16	15%	V4'
	4	16	16	16	16	15%	V4'

(b) GRADATION 8 AT PIXEL A

	A	B	C	D	E	REFLECTANCE	GRADATION SIGNAL
K21	8	1	1	1	1	34.2%	V8'
	8	1	1	1	2	34.1%	V8'
	8	1	1	2	2	34.0%	V8'
	8	1	2	2	2	34.0%	V8'
	8	2	2	2	2	33.8%	V8'
	⋮					⋮	⋮
K22	8	7	7	7	7	33%	V8
	8	7	7	7	8	33%	V8
	8	7	7	8	8	33%	V8
	8	7	8	8	8	33%	V8
	8	8	8	8	8	33%	V8
	⋮					⋮	⋮
K23	8	15	15	15	15	31.4%	V8"
	8	15	15	15	16	31.5%	V8"
	8	15	15	16	16	31.5%	V8"
	8	15	16	16	16	31.6%	V8"
	8	16	16	16	16	31.6%	V8"

FIG.4

(a) GRADATION 12 AT PIXEL A

	A	B	C	D	E	REFLECTANCE	GRADATION SIGNAL
K31	12	1	1	1	1	50.6%	V12'
	12	1	1	1	2	50.5%	V12'
	12	1	1	2	2	50.5%	V12'
	12	1	2	2	2	50.4%	V12'
	12	2	2	2	2	50.4%	V12'
	⋮					⋮	⋮
K32	12	7	7	7	7	49%	V12
	12	7	7	7	8	49%	V12
	12	7	7	8	8	49%	V12
	12	7	8	8	8	49%	V12
	12	8	8	8	8	49%	V12
	⋮					⋮	⋮
	12	15	15	15	15	48.9%	V12
	12	15	15	15	16	48.8%	V12
	12	15	15	16	16	48.8%	V12
	12	15	16	16	16	48.8%	V12
	12	16	16	16	16	48.7%	V12

(b) GRADATION 16 AT PIXEL A

	A	B	C	D	E	REFLECTANCE	GRADATION SIGNAL
K41	16	1	1	1	1	67.0%	V16'
	16	1	1	1	2	67.0%	V16'
	16	1	1	2	2	67.0%	V16'
	16	1	2	2	2	66.8%	V16'
	16	2	2	2	2	66.8%	V16'
	⋮					⋮	⋮
K42	16	7	7	7	7	65.8%	V16
	16	7	7	7	8	65.7%	V16
	16	7	7	8	8	65.7%	V16
	16	7	8	8	8	65.6%	V16
	16	8	8	8	8	65.6%	V16
	⋮					⋮	⋮
	16	15	15	15	15	65%	V16
	16	15	15	15	16	65%	V16
	16	15	15	16	16	65%	V16
	16	15	16	16	16	65%	V16
	16	16	16	16	16	65%	V16

FIG.5

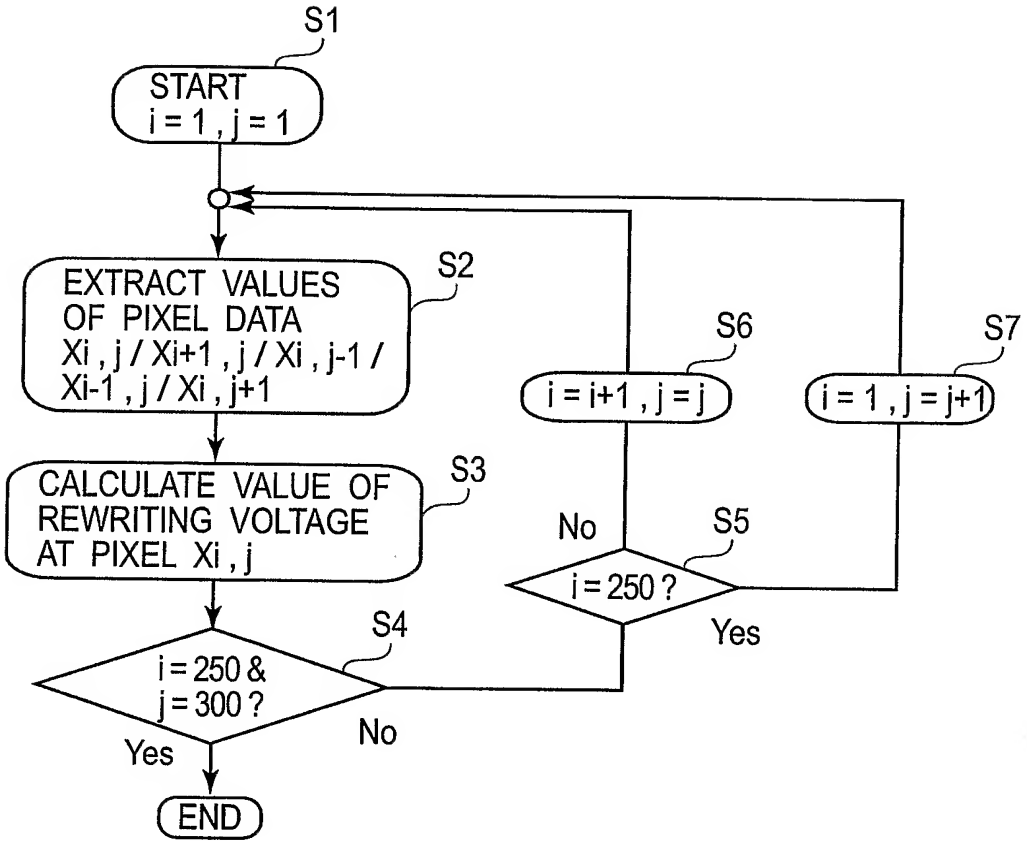

S1
START
i = 1 , j = 1
S2
EXTRACT VALUES OF PIXEL DATA Xi , j / Xi+1 , j / Xi , j-1 / Xi-1 , j / Xi , j+1
S3
CALCULATE VALUE OF REWRITING VOLTAGE AT PIXEL Xi , j
S4
i = 250 & j = 300 ?
Yes
No
END
S5
i = 250 ?
No
Yes
S6
i = i+1 , j = j
S7
i = 1 , j = j+1

FIG.6

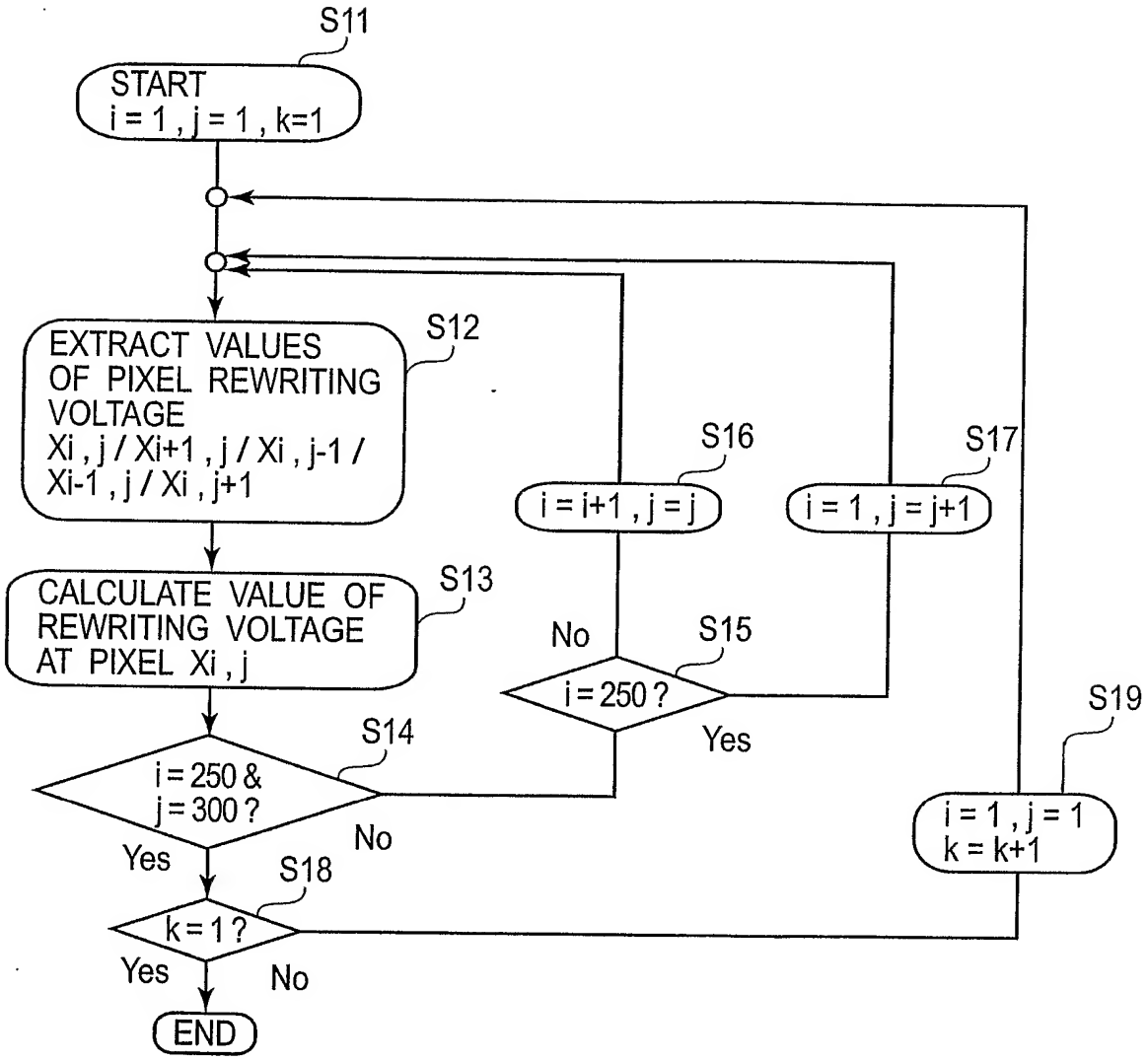

S11
START
i = 1 , j = 1 , k=1
S12
EXTRACT VALUES OF PIXEL REWRITING VOLTAGE
Xi , j / Xi+1 , j / Xi , j-1 / Xi-1 , j / Xi , j+1
S13
CALCULATE VALUE OF REWRITING VOLTAGE AT PIXEL Xi , j
S14
i = 250 & j = 300 ?
Yes
No
S15
i = 250 ?
No
Yes
S16
i = i+1 , j = j
S17
i = 1 , j = j+1
S18
k = 1 ?
Yes
No
S19
i = 1 , j = 1
k = k+1
END

FIG. 7

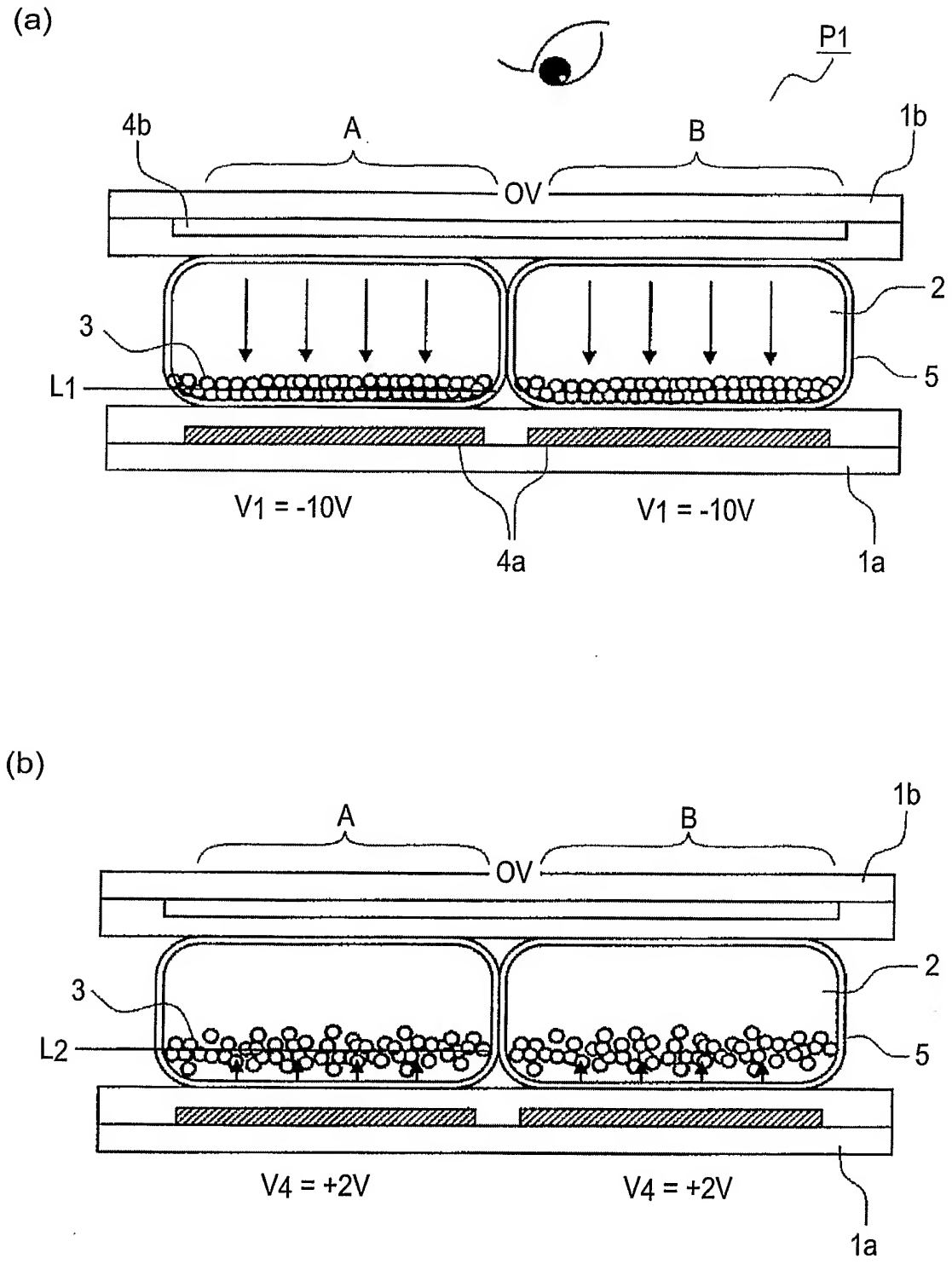

(a)
P1
4b
A
B
1b
OV
2
3
5
L1
V1 = -10V
V1 = -10V
4a
1a
(b)
A
B
1b
OV
2
3
5
L2
V4 = +2V
V4 = +2V
1a

FIG.8

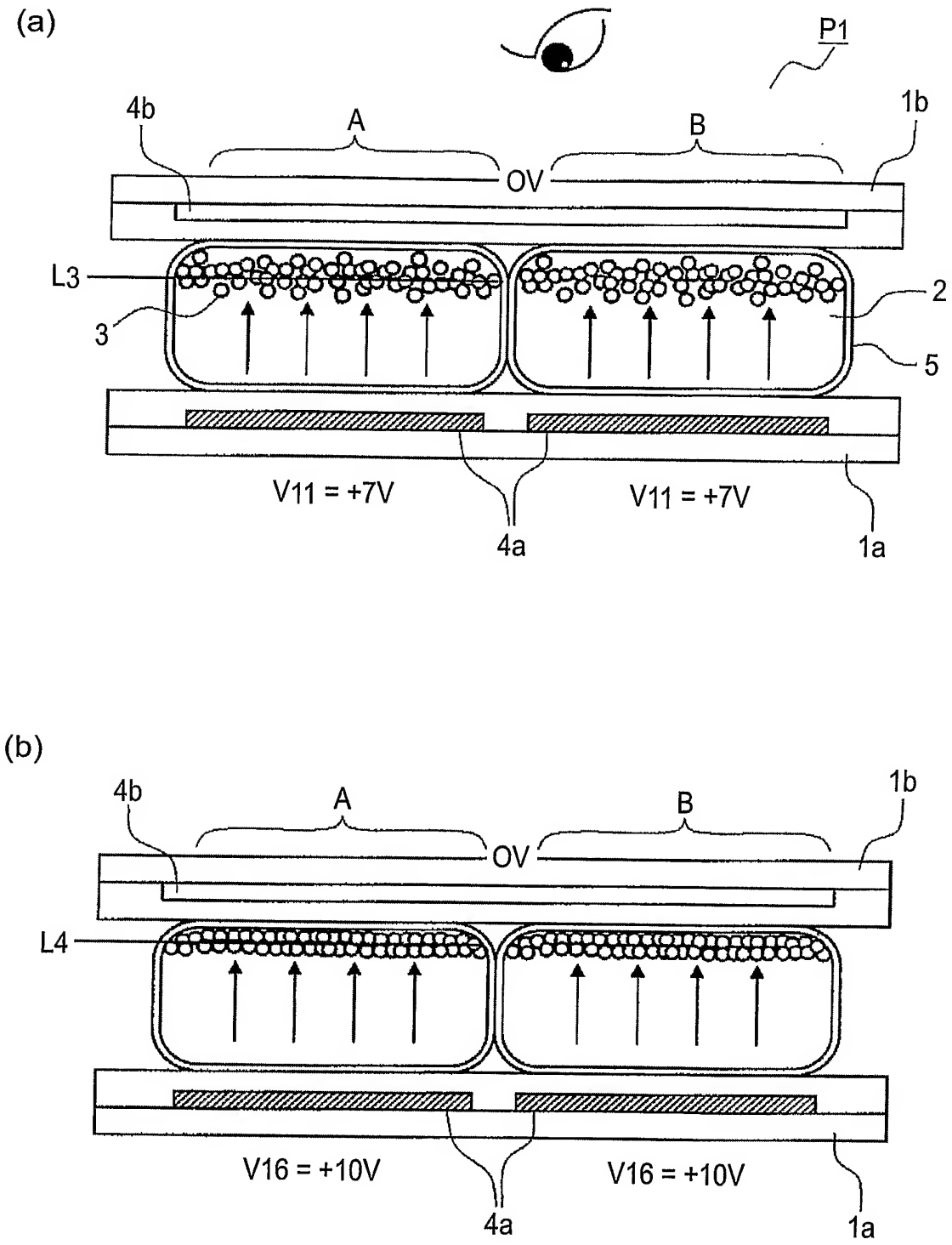
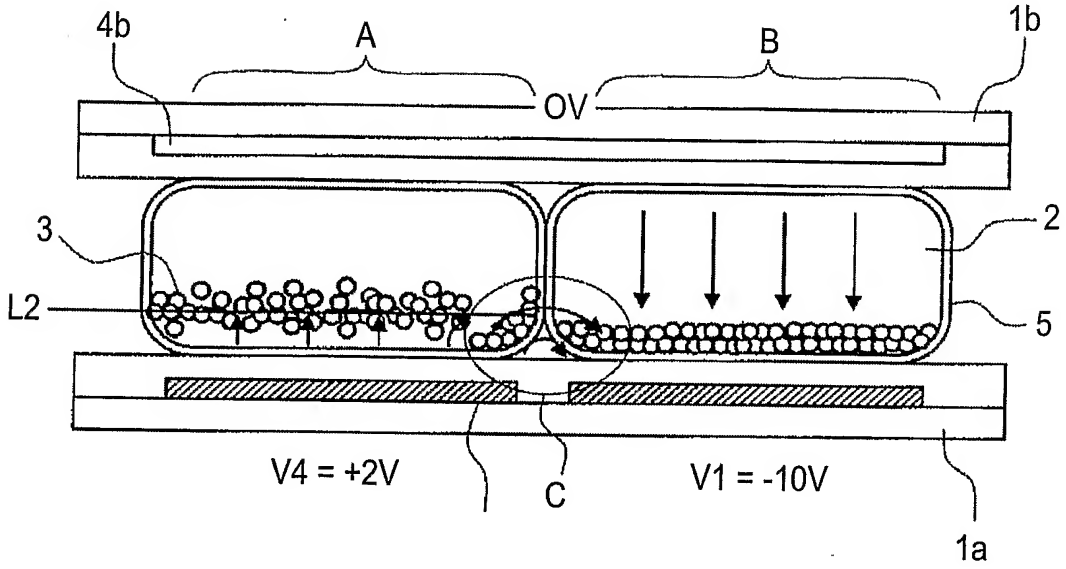

(a)
P1
4b
A
B
1b
OV
L3
3
2
5
V11 = +7V
V11 = +7V
4a
1a
(b)
4b
A
B
1b
OV
L4
V16 = +10V
V16 = +10V
4a
1a

FIG.9

(a)


4b
A
B
1b
OV
3
2
L2
5
V4 = +2V
C
V1 = -10V
1a

(b)

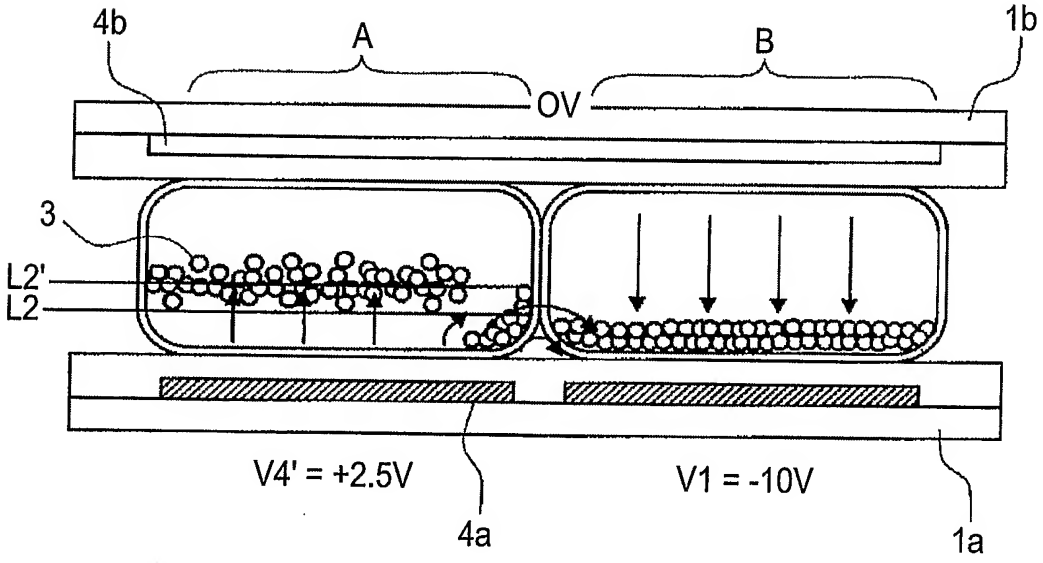

4b
A
B
1b
OV
3
L2'
L2
V4' = +2.5V
4a
V1 = -10V
1a

FIG. 10

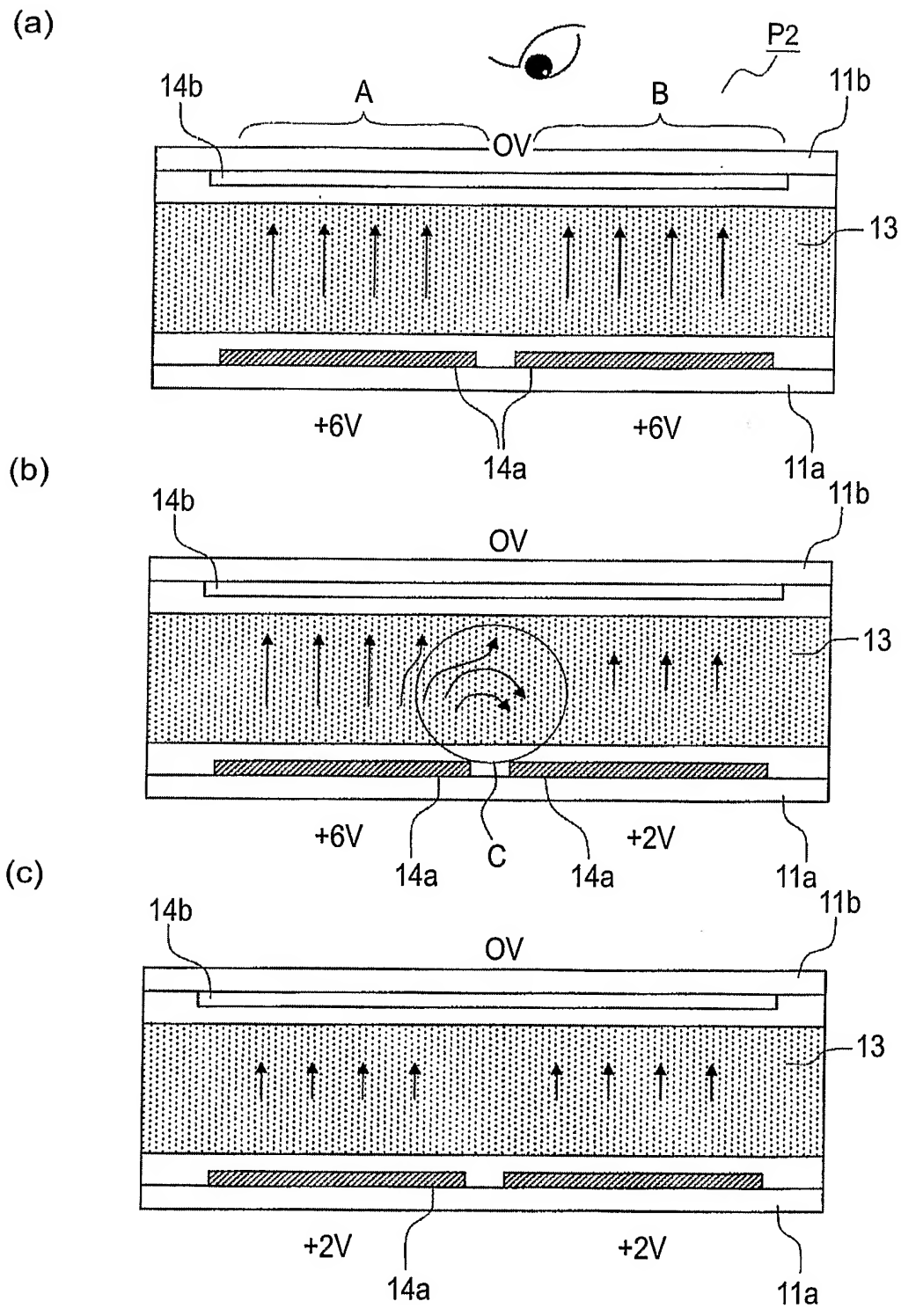
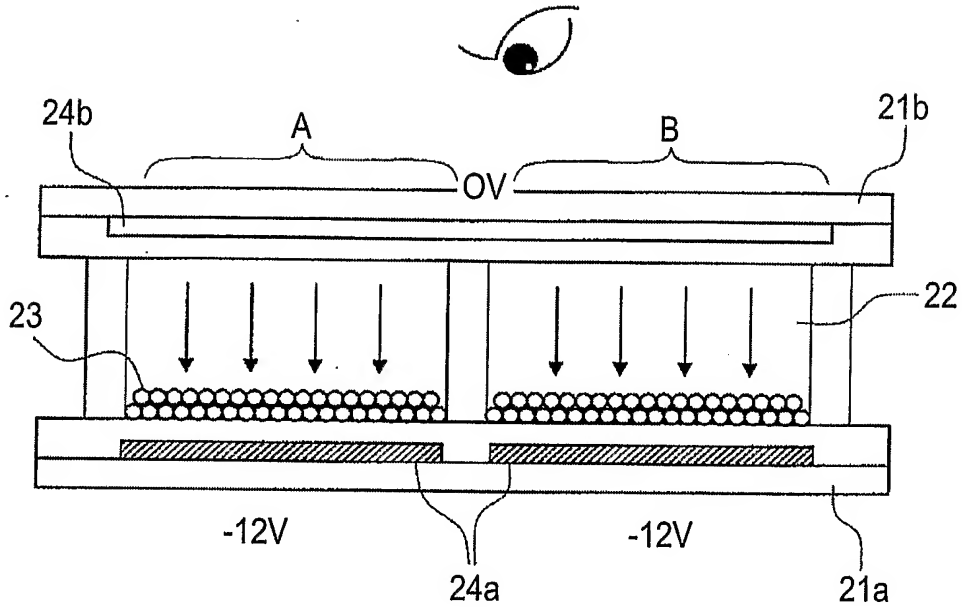

(a)
P2
14b
A
B
11b
OV
13
+6V
+6V
14a
11a
(b)
14b
11b
OV
13
+6V
C
+2V
14a
14a
11a
(c)
14b
11b
OV
13
+2V
+2V
14a
11a

FIG. 11

(a)


24b
A
B
21b
OV
22
23
-12V
-12V
24a
21a

(b)

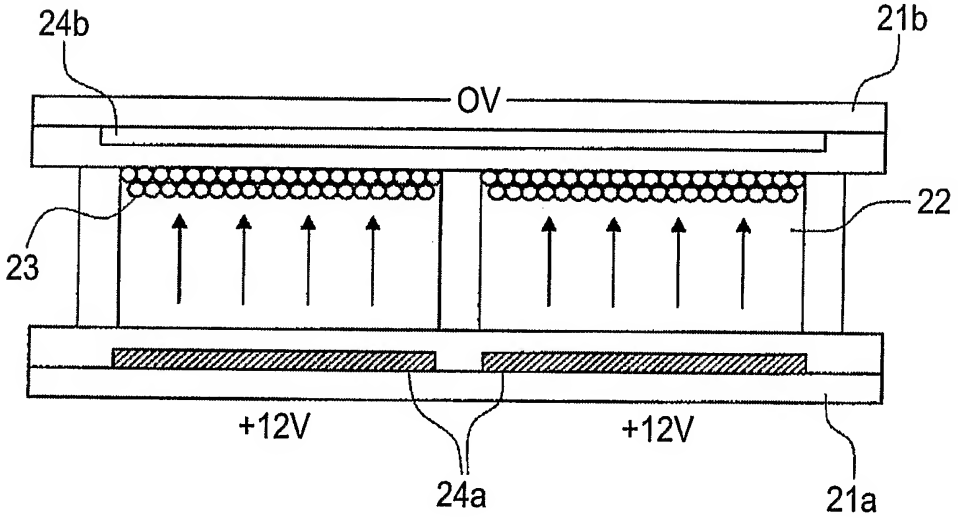

24b
21b
OV
22
23
+12V
+12V
24a
21a

FIG. 12

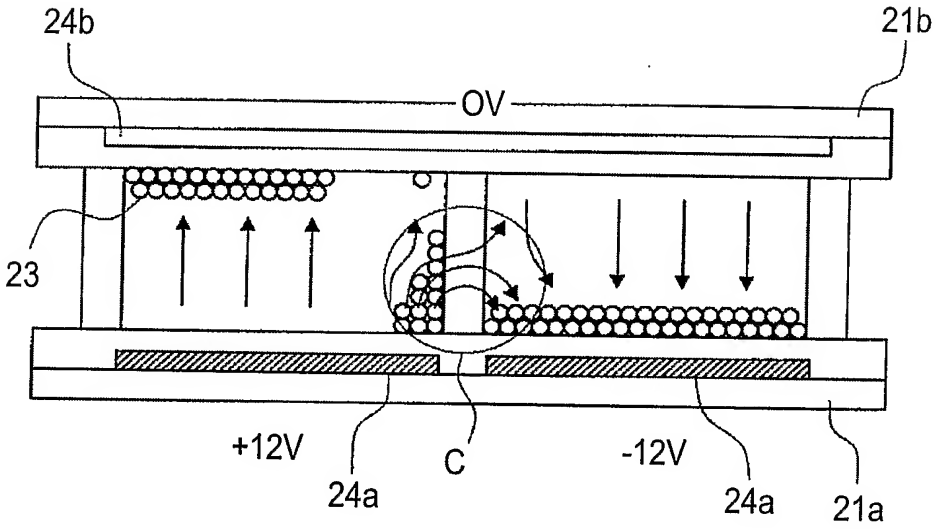


FIG. 13

INTERNATIONAL SEARCH REPORT

Int... plication No
P.., JP2004/010081

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/34 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/043180 A1 (MIURA SEISHI ET AL) 22 November 2001 (2001-11-22) paragraphs '0012!, '0039!, '0041!, '0042!, '0050!, '0054!, '0055!; figures 5,8	1-5
X	US 5 841 411 A (FRANCIS ANDREW M) 24 November 1998 (1998-11-24) column 1, line 42 - column 1, line 55; figures 1,9 column 3, line 9 - column 3, line 33 column 6, line 3 - column 6, line 23 column 8, line 16 - column 8, line 40	1-5

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
1 September 2004	16/09/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Kunze, H

INTERNATIONAL SEARCH REPORT

Int... application No
P..., JP2004/010081

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 700 028 A (SONY CORP) 6 March 1996 (1996-03-06) column 6, line 10 - column 6, line 34; figures 1,2 column 5, line 42 - column 5, line 55 column 5, line 57 - column 6, line 4 column 7, line 41 - column 7, line 49 column 6, line 26 - column 6, line 34	1-5

INTERNATIONAL SEARCH REPORT

ation on patent family members

Interpat Application No
P.., JP2004/010081

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		WO 9744774 A2	27-11-1997
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EP 0700028 A	06-03-1996	JP 3332062 B2	07-10-2002
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		DE 69521377 T2	18-04-2002
		EP 0700028 A1	06-03-1996
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